adhering top plate parallel to said arraying flat bed in relative manner thereto, thereby adhering ends of the positioned and aligned chip-style electronic components to said adhesive; and

a coating step of lowering said first film, to which the chip-style electronic components are adhered, in relative manner and together with a coating top plate parallel to a coating flat bed provided with a conductive paste layer of a constant thickness thereby pressing the other ends of the chip-style electronic components to said coating flat bed.

REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-15 are presently pending in this application, Claims 6-15 having been withdrawn from further consideration by the Examiner, and Claim 1 having been amended by the present amendment.

In the outstanding Office Action, the drawings were objected to because of informalities; Claims 1-5 were rejected under 35 U.S.C. §102(b) as being anticipated by Minowa et al. (U.S. Patent 5,622,585); and Claims 1-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nitta et al. (U.S. Patent 4,664,943) in combination with JP 11-334785A (hereinafter "JP '785") or Minowa et al.

In response to the objection to the drawings, submitted herewith is a separate LETTER REQUESTING APPROVAL FOR DRAWING CHANGES, submitting for approval changes to Figures 11-15. Specifically, Figures 11-15 have been amended to add the legend "Prior Art" as required by the Examiner.

Claim 1 has been amended solely to correct a typographical informality, and thus the claim amendment is not believed to narrow the scopes of the claims.

Briefly recapitulating, Claim 1 according to the present invention is directed to a terminal electrode forming method for chip-style electronic components, including an arraying step of arraying the chip-style electronic components on an arraying flat bed thereby positioning and aligning said chip-style electronic components, an adhering step of lowering a first film coated with an adhesive together with an adhering top plate parallel to said arraying flat bed in relative manner thereto, thereby adhering ends of the positioned and aligned chip-style electronic components to said adhesive, and a coating step of lowering said first film, to which the chip-style electronic components are adhered, in relative manner and together with a coating top plate parallel to a coating flat bed provided with a conductive paste layer of a constant thickness thereby pressing the other ends of the chip-style electronic components to said coating flat bed. As such, the electronic components aligned on an arraying flat bed are adhered to a film coated with an adhesive. In doing so, the adhering top plate parallel to the arraying flat bed is utilized for pressing the electronic components to the arraying flat bed. Also, in the coating step, the film to which the electronic components are adhered are lowered toward a coating flat bed provided with a conductive paste layer so that conductive paste is applied to the other ends of the electronic components. In doing so, the coating top plate is utilized for pressing the electronic components to the coating flat bed.

Some advantages attributable to the method according to Claim 1 are as follows. Transfer of the components between the sites of consecutive steps can be simplified, since the transfer is attained only by transferring the film to which the electronic components are attached. For example, the transfer can be attained by using the film in the form of a tape and using feeding and winding rolls to move the film tape. Also, the film is disposable, since it is

made of an inexpensive resin film such as a PET (polyethylene terephthalate) film.

Minowa et al. disclose a method of handling electronic component chips. Nevertheless, it is respectfully submitted that Minowa et al. are not believed to teach "an adhering step of lowering a first film coated with an adhesive together with an adhering top plate parallel to said arraying flat bed in relative manner thereto, thereby adhering ends of the positioned and aligned chip-style electronic components to said adhesive; and a coating step of lowering said first film, to which the chip-style electronic components are adhered, in relative manner and together with a coating top plate parallel to a coating flat bed provided with a conductive paste layer of a constant thickness thereby pressing the other ends of the chip-style electronic components to said coating flat bed" as recited in Claim 1. According to Claim 1, the electronic components are adhered to a film, e.g., a film made of PET as described in the specification, coated with an adhesive, and separate plates, i.e., the adhering top plate in the adhering step and the coating top plate in the coating step, are utilized for pressing. Schematically, the structure according to Claim 1 would be illustrated as [film+adhesive] / [separate plate], whereas the structure disclosed in Minowa et al. would be illustrated as [body plate+adhesive]. According to the Minowa et al. method, electronic components are adhered to an adhesive film 23 formed on a plate-like, i.e., rigid, body 22 made of a material such as a metal or resin. Minowa et al. state that "[t]he adhesive film 23 may be independently formed in another place, and then pasted on the body 22" and that "[a]lternatively, the adhesive film 23 may be formed on the body 22."[1] That is, the adhesive film 23 in Minowa et al. refers to an adhesive layer that is directly applied or attached to the plate-like body 22, and the adhesive film 23 is adhesive itself and made integral with the plate-like body 22. Therefore, the body 22 is carried to the next process, e.g., a step of

[1] Minowa et al., column 5, lines 30-32.

coating electrode paste together with the electronic components.[2] The adhesive film 23 in Minowa et al. refers to the adhesive layer itself, and there is no film apart from the adhesive. As discussed above, according to Claim 1, the film may be disposed of. In contrast, in the Minowa et al. method, the plate-like body 22 is not disposable, but should be used repeatedly, requiring a cleaning process of the adhesive film 23 remaining on the body 22, when the adhesive film is cured. On the basis of these discussions, Applicants respectfully submit that the subject matter recited in Claim 1 is believed to be clearly distinguishable from Minowa et al.

Nitta et al. merely discloses a method for forming electrodes of electronic component chips, and JP '851 discloses a use of a thermally releasable adhesive tape for holding or transferring. However, neither Nitta et al. nor JP '851 teaches "an adhering step of lowering a first film coated with an adhesive together with an adhering top plate parallel to said arraying flat bed in relative manner thereto, thereby adhering ends of the positioned and aligned chip-style electronic components to said adhesive; and a coating step of lowering said first film, to which the chip-style electronic components are adhered, in relative manner and together with a coating top plate parallel to a coating flat bed provided with a conductive paste layer of a constant thickness thereby pressing the other ends of the chip-style electronic components to said coating flat bed" as recited in Claim 1. Notably, Nitta et al. are not believed to disclose or suggest any part of the subject matter recited in Claim 1, and JP '851 does not relate to forming of electrodes on electronic components, and are not believed to disclose the subject matter recited in Claim 1 either. Hence, the subject matter recited in Claim 1 is believed to be clearly distinguishable from both Nitta et al. and JP '851.

Because none of Minowa et al., Nitto et al. And JP '851 discloses the adhering and

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[2] See Minowa et al., column 6, lines 21- .

coating steps as recited in Claim 1, even the combined teachings of these cited references are not believed to render the subject matter recited in Claim 1 obvious.

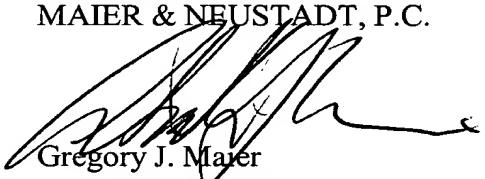
For the foregoing reasons, Claim 1 is believed to be allowable. Furthermore, since Claims 2-5 ultimately depend from Claim 1, substantially the same arguments set forth above also apply to these dependent claims. Hence, Claims 2-5 are believed to be allowable as well.

In addition, Applicants wish to point out that none of the cited references discloses or suggests the subject matters recited in Claims 3 and 4, namely, transfer of the film in the form of a tape performed by feeding and winding rolls, and use of far-infrared light in the drying step, respectively. Conventionally, the drying of conductive paste has been performed in a heated atmosphere at about 180°C, which would bring about deformation of a resin film. The irradiation of far-infrared light does not cause such a deformation.

In view of the amendments and discussions presented above, Applicants respectfully submit that the present application is in condition for allowance, and an early action favorable to that effect is earnestly solicited.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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Please amend Claim 1 as follows:

--1. (Amended) A terminal electrode forming method for chip-style electronic [componens] components, comprising:

an arraying step of arraying the chip-style electronic components on an arraying flat bed thereby positioning and aligning said chip-style electronic components;

an adhering step of lowering a first film coated with an adhesive together with an adhering top plate parallel to said arraying flat bed in relative manner thereto, thereby adhering ends of the positioned and aligned chip-style electronic components to said adhesive; and

a coating step of lowering said first film, to which the chip-style electronic components are adhered, in relative manner and together with a coating top plate parallel to a coating flat bed provided with a conductive paste layer of a constant thickness thereby pressing the other ends of the chip-style electronic components to said coating flat bed.--